What is claimed is:

1. A multilevel wiring interconnect in an integrated circuit, comprising:

a number of multilayer metal lines connecting to a number of silicon devices in a substrate;

a low dielectric constant insulator in a number of interstices between the number of multilayer metal lines and the substrate; and

wherein the low dielectric constant insulator includes a number of air gaps in the low dielectric constant material.

2. The multilevel wiring interconnect of claim 1, wherein the low dielectric constant insulator includes a low dielectric constant organic silica film.

3. The multilevel wiring interconnect of claim 1, wherein the low dielectric constant insulator includes a low dielectric constant insulator having a dielectric constant (k) of less than 2.7.

4. The multilevel wiring interconnect of claim 1, wherein the low dielectric constant insulator includes a film in which of a set of methyl groups and a flourine group of atoms are as much as 43% and 9% respectively of that for a content of silicon atoms in the film.

5. The multilevel wiring interconnect of claim 1, wherein the number of multilayer metal lines includes a number of multilayer metal lines selected from the group consisting of Aluminum, Copper, Silver, and Gold.

6. The multilevel wiring interconnect of claim 1, wherein the number of multilayer metal lines includes a first conductor bridge level.

7. A multilevel wiring interconnect system, comprising:

a number of multilayer metal lines connecting to a number of integrated circuit devices in a substrate; and

a low dielectric constant insulator in a number of interstices between the number of multilayer metal lines and the substrate, the low dielectric constant insulator having a number of air gaps therein.

8. The system of claim 7, wherein the number of multilayer metal lines are adapted to connect to at least one of a processor and a memory.

9. The system of claim 7, wherein the substrate is a die.

10. The system of claim 7, wherein the substrate includes a silicon.

11. The system of claim 7, wherein the number of multilayer metal lines consist essentially of copper.

12. A system having a multilevel wiring interconnect, comprising:

an integrated circuit device; and

an integrated memory circuit operably coupled to the integrated circuit device, wherein the integrated memory circuit includes a multilevel wiring interconnect, the multilevel wiring interconnect comprising:

a number of multilayer Copper lines connecting to one or more of the transistors in the substrate;

a low dielectric constant insulator in a number of interstices between the number of multilayer Copper lines and the substrate; and

wherein the low dielectric constant insulator includes a number of air gaps in the low dielectric constant material.

13. The system of claim 12, wherein the integrated circuit device includes a processor.

14. A system, comprising:

a processor; and

an integrated memory circuit coupled to the processor, wherein the integrated memory circuit further includes a multilevel wiring interconnect, the multilevel wiring interconnect comprising:

a number of multilayer Copper lines connecting to one or more of the transistors in the substrate;

a low dielectric constant insulator in a number of interstices between the number of multilayer Copper lines and the substrate; and

wherein the low dielectric constant insulator includes a number of air gaps in the low dielectric constant material.

15. The system of claim 14, wherein the low dielectric constant insulator includes a low dielectric constant organic silica film.

16. The system of claim 14, wherein the low dielectric constant insulator includes a low dielectric constant insulator having a dielectric constant of less than 2.7.

17. The system of claim 16, wherein the low dielectric constant insulator includes a film in which of a set of methyl groups and a flourine group of atoms are as much as 43% and 9% respectively of that for a content of silicon atoms in the film.